IN THE CLAIMS

1. (Currently amended) An instruction processing apparatus, comprising: an instruction memory ~~(10)~~; an instruction addressing unit ~~(11)~~ coupled to supply instruction addresses to the instruction memory ~~(10)~~; instruction processing circuitry ~~(12)~~ coupled to receive and execute addressed instructions from the instruction memory ~~(10)~~, the instructions including branch instructions, the instruction processing circuitry ~~(12)~~ being coupled to the instruction addressing unit ~~(11)~~ to control the instruction addresses in response to the branch instructions; an activity monitor ~~(16)~~ for monitoring activity in at least a part of the apparatus during execution of the instructions, and for supplying measures of activity that occur during execution of instructions following the respective ones of the branch instructions; an activity table memory ~~(140)~~ coupled to the activity monitor ~~(16)~~, the activity table memory ~~(140)~~ being arranged to store entries that record information about the measures of activity associated with the respective ones of the branch instructions respectively.

2. (Currently amended) An instruction processing apparatus according to claim 1, wherein the activity table memory ~~(140)~~ is arranged to capture information about the measured activity during execution of instructions starting from an instruction executed after the branch instruction at least until a next executed branch instruction.

3. (Currently amended) An instruction processing apparatus according to claim 1, comprising a mode select unit ~~(18)~~ for controlling a mode of operation of the processing circuitry ~~(12)~~ that affects power consumption by the processing circuitry ~~(12)~~, the activity

table memory ~~(140)~~ having an output coupled to the mode select unit ~~(12)~~ to output data derived from the information about the measure of activity for a particular one of the branch instructions, upon detection of fetching and/or execution of the particular one of the branch instructions, for controlling selection of the mode.

4. (Currently amended) An instruction processing apparatus according to claim 3, wherein the activity table memory ~~(140)~~ has locations for a predetermined number of branch instructions, the processing apparatus comprising a table memory management unit ~~(141)~~ for selecting for which of the branch instructions the entries are retained in said locations, and for directing supply of default information to the mode select unit ~~(18)~~ when no information has been retained for the particular one of the branch instructions.

5. (Currently amended) An instruction processing apparatus according to claim 1, wherein the activity table memory ~~(140)~~ is arranged to retain information about the measure of activity for both the case when the branch is taken and when the branch is not taken respectively, the processing-circuitry signaling which information should be updated dependent on the outcome of the branch.

6. (Currently amended) An instruction processing apparatus according to claim 5, comprising a mode select unit ~~(18)~~ for adapting a mode of operation of the processing circuitry that affects power consumption by the processing circuitry, the activity table memory ~~(140)~~ having an output coupled to the mode select unit ~~(18)~~ to output data derived from the information about the measure of activity for a particular one of the

branch instructions, upon detection of fetching and/or execution of the particular one of the branch instructions, for controlling selection of the mode, the information being selected dependent on whether the particular one of the branch instructions is taken or not.

7. (Currently amended) An instruction processing apparatus according to claim 1, wherein the activity table memory ~~(140)~~ is part of a branch prediction unit ~~(14)~~, information about a frequency with which the respective ones of the branch instructions are taken being recorded in said entries, for predicting whether the branch instructions, when encountered subsequently, will be taken.

8. (Currently amended) A method of executing a program of instructions, the method comprising detecting the execution of branch instructions; determining respective measures of activity of processing circuitry ~~(12)~~, each measure of activity during execution of instructions following a respective one of the branch instructions in response to detection of the branch instructions; recording information about the respective measures of activity in association information that identifies the respective one of the branch instructions.

9. (Previously presented) A method of executing a program of instructions according to claim 8, the method comprising using the information about the recorded measures of activity to select respective power consumption setting modes to be used during execution of at least part of the instructions following the respective ones of the branch

instructions.

10. (Previously presented) A method of executing a program of instructions according to claim 9, wherein said selecting respective power consumption setting modes is performed statically, in advance of execution of the program, using accumulated measures of activity from a previous run of the program for respective blocks of instructions following respective ones of the branch instructions.

11. (Previously presented) A method of executing a program of instructions according to claim 9, wherein said selecting respective power consumption setting modes is performed dynamically during execution of the program, dependent on current information about the measure of activity for instructions following a particular one of the branch instructions.